MODEL 2412A BUFFER MEMORY

OPERATION AND INSTALLATION MANUAL

Revision 2.1
September 1986

The material in this manual is for informational purposes only and is subject to change without notice.

Part No. 9000-0460

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1. INTRODUCTION

The Model 2412A Buffer Memory is a 4096-channel one- or two-dimensional alternately-paged data acquisition buffer designed specifically for use with Model 2391 and 2401 Position Computers. The Model 2412A Buffer Memory functions as a temporary data accumulation buffer and interface between the position computer (and associated sensor) and a host computer that controls the data accumulation. This configuration frees the host computer for tasks other than data acquisition and, in some cases, enables higher effective count rates than can be accepted by the host computer directly. Communication between the Model 2412A Buffer Memory and the host computer is via two uni-directional parallel data buses.

This manual consists of 4 major sections plus appendices. The appendices are intended primarily for reference and need not be read in order to understand the operation of the Model 2412A Buffer Memory. The remaining major sections contain basic information relating to the operation, programming, and interfacing of the Model 2412A and should be read by all users. It is assumed that the reader is already familiar with the operation of the Model 2391 or Model 2401 Position Computer to which the Buffer Memory is to be connected.

The Model 2412A is available with two different host computer interfaces. The 2412-01 is compatible with Digital Equipment Corporation (DEC) General Device Interfaces, including the DR11-C for Unibus and DRV-11 for Q-bus applications. The 2412-02 is compatible

with the Hewlett Packard (HP) 98622A GPIO Interface. Unless otherwise stated, all information in this manual applies to both host computer configurations. Differences will be identified as applying to either HP or DEC interfaces.

Normally, the Buffer Memory is supplied factory-instailed in the Model 2401 Position Computer. The Buffer Memory also is available separately (2412-21 for DEC interfaces, 2412-22 for HP GPIO interface). This options allows customer installation in an existing Model 2401 or in a customer-supplied enclosure for use with the Model 2391 Position Computer or other custom applications. All options include cables for connecting the Buffer Memory to an appropriate host computer interface.

Table 1 provides a summary of the specifications for the Model 2412A Buffer Memory.

Table 1◦ Model 2412A Buffer Memory specifications summary.

Memory size:	Two pages of 4096 words each
Word size:	16 bits (0 - 65,535' counts)
Data Input or Output Cycle time:	0.35 - 0.70 microseconds$_z$ dependent upon overlap of input and output requests
Data rate :	0-1 MHz, input and output combined
Programmable Timer:	Range: 1 to 32,767 milliseconds Resolution : 1 millisecond
Programmable Functions :	Set timer Start accumulation Stop accumulation
Inputs to 2412A from Position Computer :	10 bits X position, 10 bits Y position, TTL compatible ; strappable for 1—12 bits total address
2412-01, 2412-21 host computer interface:	Digital Equipment Corp. DRV-11 or DR-11C General Device Interface
Inputs to 2412A:	16 data lines, NEW DATA RDY, DATA TRANS, INIT; TTL compatible
Outputs to hosts	16 data lines, REQUEST A ; TTL compatible
2412-02, 2412-22 host computer interface:	Hewlett Packard 98622A GPIO Interface
Inputs to 2412A:	16 data lines, PCTL, I/O, PRESET ; TTL compatible
Outputs to host:	16 data lines, PFLG, PSTS, STIO; TTL compatible
Power required:	5 Volts DC @ 1.0 amp
Dimensions:	6.5" by 10.0** (Can be installed in Model 2401 Position Computer)
Weight:	Net: Approximately 0.5 lbs (0.3 kg) Shipping: Approximately 2.0 lbs (0.9 kg)

2. MODEL 2412A OVERVIEW

2.1. Principles of Operation

Figure 1 illustrates a typical system configuration. For each electron striking the sensor, the position computer generates analog X and Y output voltages whose magnitudes correspond to the X and Y coordinates of the incident electron. Digital representations of these voltages are combined to form an input word (maximum of 12 bits) to the Buffer Memory and the content of the corresponding channel (memory location addressed by the input word) in the Buffer Memory is then incremented by one count to represent the sensor event. Depending upon the specific input connections to the Model 2412A, the Buffer Memory may be used to accumulate only X or only Y coordinate data or a combination of X and Y data. A maximum of 12 bits of X and/or Y coordinate data may be used, corresponding to 4096 data channels.

Following completion of data accumulation, the host computer serially reads the contents of the Buffer Memory channels. Since each memory channel corresponds to a specific combination of X and/or Y coordinate data, each value read corresponds to the number of incident events at a specific sensor X-Y position. If the Buffer Memory was used as a one-dimensional buffer, the data provides a distribution (in the selected axis) of the sensor events. In the two-dimensional mode, the data may be used to create an image relating intensity (number of counts) to X-Y position.

Data accumulation can occur in two modes: timed and untimed. Specific time periods can be set by programming the on-board timer from the host computer. Settable time periods range from 1 millisecond to 32767 milliseconds in 1 millisecond intervals. The timed mode provides very precise control of total accumulation time, while allowing the host computer to perform other functions during data accumulation. It is also useful in scanning applications where all scan increments are to be collected for the same time period. At the completion of a timed accumulation cycle$_z$ the Buffer Memory issues a request for service to the host computer. The timer automatically resets at the end of an accumulation cycle, so the on-board timer needs to be reset prior to a new accumulation cycle only if the time period is to be changed from its previous value.

If the on-board timer is set to zero, a data accumulation cycle will continue until the host computer issues a stop command. In this mode, the Buffer Memory issues a request for service once any channel is completely full (65_z535 counts). Data accumulation is not stopped by the request for service, but full channels will not overflow with additional counts.

After setting the timer, an accumulation cycle (timed or untimed) is begun by the host computer issuing a start command to the Buffer Memory. The single light-emitting diode on the Buffer Memory board is lit during the accumulation cycle. The specific form of the service request generated at the end of a timed cycle or when a memory channel is full differs for the HP and DEC interfaces; refer to Section 4 of

this manual for details.

The Model 2412A Buffer Memory contains two 4096 word buffers, one for input and one for output. These alternately-paged buffers allow data accumulation to occur concurrently with the host computer reading the data from the previous accumulation. The buffers are swapped at the start of each accumulation cycle. The input buffer is only active during the accumulation cycle; i.e., for the period of time specified by the on-board timer. The output buffer can be accessed at any time and each output buffer channel is cleared (set to zero) when it is read by the host computer. The output buffer address pointer is automatically reset to channel zero when the buffers are swapped; successive read operations access successive output buffer channels.

2.2. X-Y Input Mapping

The relationship between the 4096 memory channels in each buffer and the X and Y coordinates of sensor events is determined by a set of wire-wrap jumpers on the 2412A board. The 12-bit input to the Model 2412A can be arbitrarily partitioned between the X and Y outputs from the Position Computer. The Model 2401 Position Computer provides a maximum of 10 bits for each dimension; the Model 2391 provides a maximum of 8 bits.

For an 8-bit resolution system, the values of X and Y can range between 0 and 255. Figure 2 illustrates how the location of an electron striking the sensor surface is translated into X and Y coordinate

values. Note that these X and Y values effectively divide the sensor surface into a set of 65,536 (256 x 256) image elements. For a 10-bit sensor, the maximum X and Y values would be 1023 instead of 255 and the surface is divided into 1,048,576 (1024 x 1024) image elements. The physically usable area of the sensor is limited by the circular shape of the microchannel plates used in construction of the sensor. The X and Y position values, however, are derived for a rectangular coordinate system, as illustrated in Figure 2.

The default configuration of the Model 2412A Buffer Memory (as shipped from the factory) is intended for use with an 8-bit resolution system. The most significant 4 bits (4 - 7) of the X-axis input are mapped into the most significant 4 bits (8 - 11) of the Buffer Memory channel address. All 8 bits (0 — 7) of the Y-axis input are mapped into the least significant 8 bits (0 - 7) of the Buffer Memory channel address. Note that the sensor image elements corresponding to each memory location are not square, but rectangular with an X dimension 16 times as long as the Y dimension. This occurs because the least significant 4 bits of the X coordinate are not used in forming the Buffer Memory channel address. Table 2 summarizes the relationship between the Buffer Memory channels and the X and Y position coordinates for the default mapping and an 8-bit resolution system.

Table 2◦ Default X-Y input mapping relationship between Buffer Memory channels and X-Y position coordinates for 8-bit resolution system•

Channel Number	Position Coordinates X	Y
0	0 ■ 15	0
1	0 - 15	1
• • •		• • •
254	0 — 15	254
255	0 ■ 15	255
256	16 — 31	0
257	16 - 31	1
•..		-• •
3838	224 - 239	254
3839	224 - 239	255
3840	240 — 255	0
3841	240 - 255	1
-• •		• •»
4094	240 — 255	254
4095	240 — 255	255

If a 9-bit or 10-bit resolution system is used or if some other X-Y input mapping is desired, then the default wire-wrap connections must be changed. Other typical mappings include 8 bits Y-axis, 0 bits X-axis; 6 bits X-axis, 6 bits Y-axis; and 10 bits Y-axis, 2 bits X-axis. Detailed instructions for changing the X-Y input mapping are provided in Appendix A of this manual. The appendix also describes several common input mappings and lists the required wire-wrap connections and channel-coordinate relationships for each.

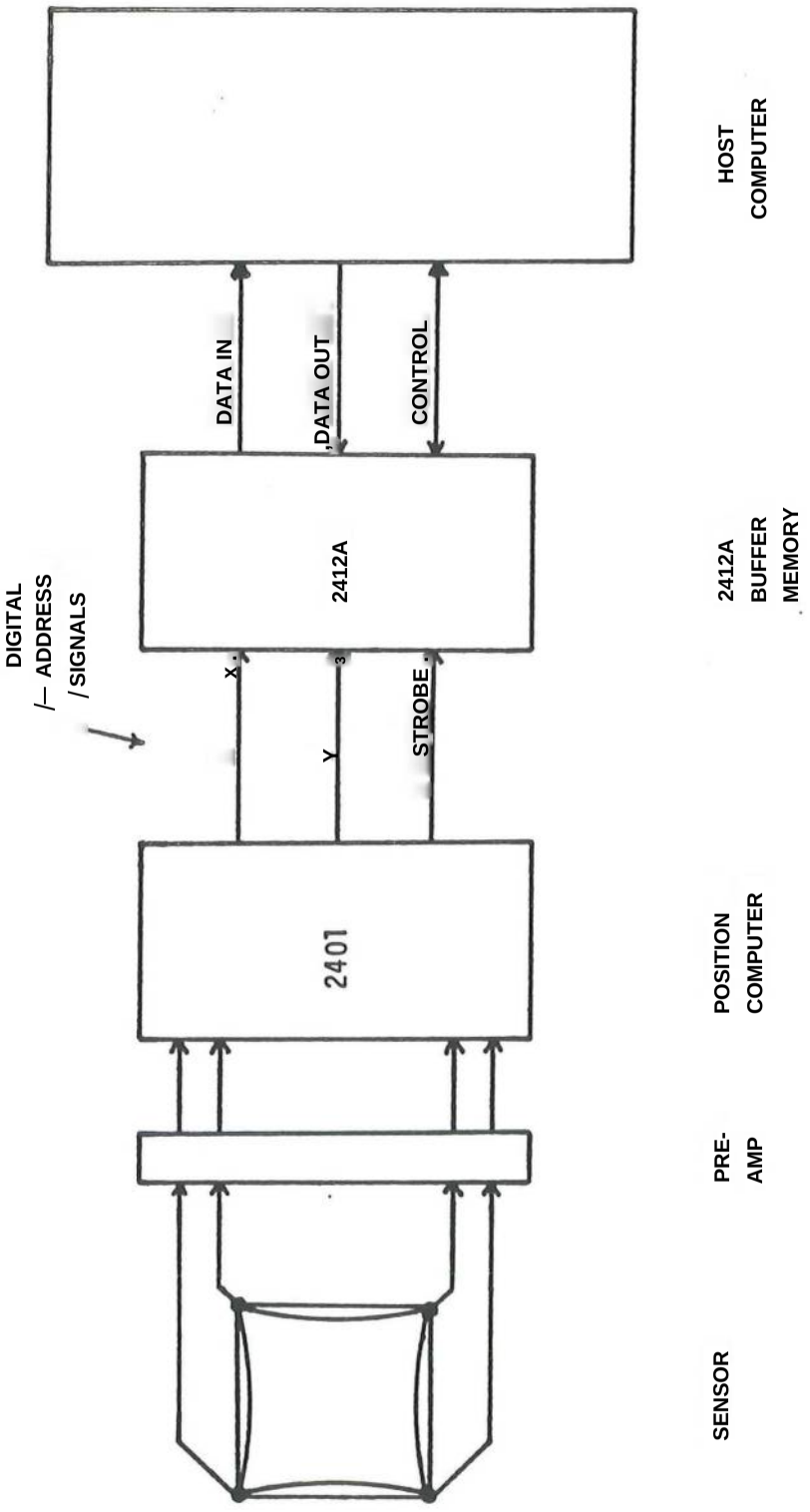


Figure 1. Block diagram of typical system configuration

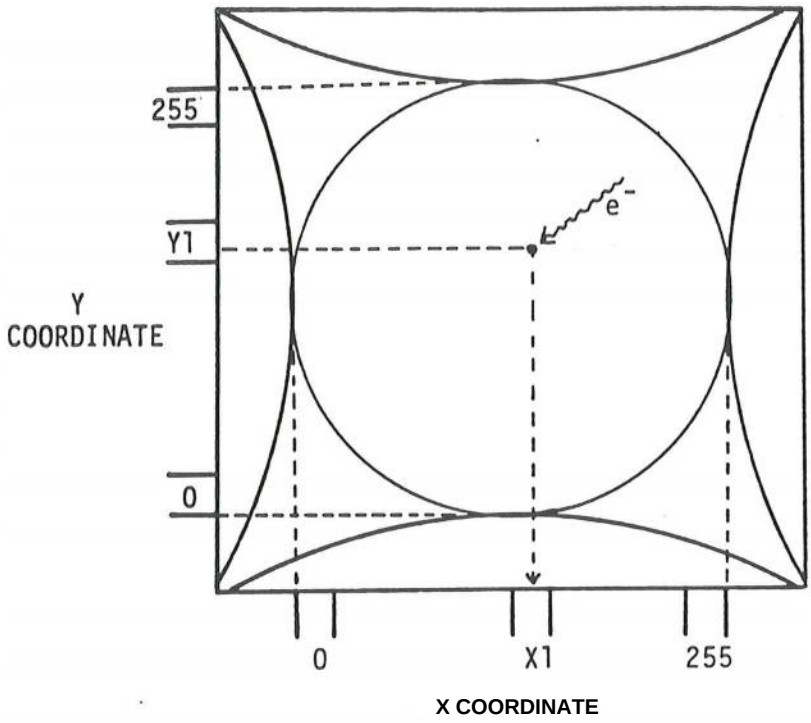


Figure 2. X and Y coordinates of sensor events (8-bit resolution).

3. PROGRAMMING THE 2412A BUFFER MEMORY

3.1. Accumulation Functions

Three commands are provided that allow the host computer to control the accumulation of data by the Model 2412A Buffer Memory. These commands allow the user to set the on-board timer, start data accumulation (and swap the buffers), and stop accumulation.

All of the commands consist of a single 16-bit word written to the 2412A Buffer Memory from the host computer. The command formats are as follows:

15 bit 0

Onnnnnnnnnnnnnnn	**Set Timer.** The "set timer" mode is specified by setting bit 15 to "0". The remaining bits (14 - 0) of this command are loaded into the on-board timer and represent the accumulation time period in milliseconds. Thus, the command (in binary) 0000001111101000 (decimal 1000) would set an accumulation time of 1 second (1000 milliseconds). If the timer is set to zero, data accumulation will occur in the untimed mode.
lxxxxxxxxxxxxxx0	**Stop Accuaulation.** This command is specified by setting bit 15 to "1" and bit 0 to "0". This command stops any data accumulation in progress, but does not swap the input and output buffers or change the output buffer address pointer.
lxxxxxxxxxxxxxx1	**Start Accumulation.** This command is specified by setting both bit 15 and bit 0 to "1". This command starts data accumulation (in either timed or untimed mode as determined by the contents of the on-board timer). The input and output buffers are swapped and the output buffer address pointer is reset to channel zero prior to the start of data accumulation.

3.2. Data Output

The Model 2412A Buffer Memory has been designed to minimize the software required to transfer data to the host computer. The input and output buffers are swapped and the output buffer address pointer is automatically reset to channel zero at the start of each accumulation cycle. Data output is not affected by the end of an accumulation cycle. The output buffer is intended to be read as a block, starting at channel 0 and continuing sequentially to channel 4095. If fewer than 12 bits are used in forming the Buffer Memory channel address, it is not necessary to read the unused high address portion of the output buffer. Note that a particular channel in the output buffer can only be read once (in sequence) for each accumulation cycle as no provision is made for resetting the address pointer except by starting a new accumulation cycle.

Data readout from the Buffer Memory is always destructive; i.e., as data is read from an output buffer channel, the content of that channel is reset to zero. If the output buffer is not read, the contents of the buffer will remain when it is swapped to become the input buffer and the new accumulation data will be added to the existing data. No other provisions have been made for clearing the buffers, thus two dummy reads should be made, one for each buffer, before starting the first data accumulation. This is illustrated in the program examples that follow.

3.3. Software Guidelines and Examples

This section includes two examples of program segments intended to illustrate communication between the Model 2412A Buffer Memory and a host computer. The examples are not intended to illustrate all possible accumulation modes or methods of host computer control, but rather to provide guidelines for the development of user programs.

The first program segment illustrates control of the Model 2412A Buffer Memory using the HP 98622A GPIO Interface (assumed to be located at select code 12 in the HP computer) . The program segment is written in HP Series 9000 BASIC. Both untimed and timed accumulation cycles are shown. The program example uses the BASIC language ENTER statement to read the data from the Buffer Memory; for time-critical applications this would probably be replaced by an assembly language routine. The major sections of this program example are as follows:

lines

1-4 These lines reserve storage for an internal data buffer and define the command words to start and stop accumulation.

5-10 These lines read in the current output buffer, swap the buffers, and read in the second buffer. This clears the buffers prior to use for data accumulation.

11-12 Line 11 starts an untimed accumulation (the timer was set to zero in line 7). The user code, for example, might control an

external device that generates events being recorded by the sensor and Buffer Memory. Line 12 stops this accumulation cycle.

13-15 These lines swap the buffers and read in the data from the untimed accumulation cycle. The user code can then analyze and/or store this data.

16-20 The on-board timer is set to 1 second and the first timed accumulation cycle is started. Note that for a timed cycle, the Buffer Memory start accumulation command is loaded into the GPIO data output register (line 18) and the PCTL line is set (line 19) to cause the 2412A to read the command. For additional information on interface protocols refer to Section 4 of this manual or to the GPIO manual. Line 20 enables response to the interrupt that will be generated when the timed accumulation cycle is completed. The destination of this interrupt was defined in line 16 to be the subroutine Readbuffer.

21-26 These lines are the interrupt service routine that is called at the end of each timed accumulation cycle. Lines 22-23 start the next accumulation cycle and swap the buffers. In a typical spectrometer application, for example, this routine would update the scan conditions prior to this command. The data from the previous accumulation cycle is read out from the Buffer Memory while the newly started accumulation cycle is in progress. After processing the data, the interrupt is re-enabled in line 25 for the current accumulation cycle.

```
 1    INTEGER D(0:4095)                          ! Data buffer in memory
 2    INTEGER Startcode,Stopcode
 3    Startcode=-32768+1                         ! Set bits 15 and 1
 4    Stopcode=-32768                            ! Set bit 15

 5    CONTROL 12,0;1                             ! Reset GPIO Interface at
                                                   select code 12
 6    ENTER 12 USING "#,W";D(*)                  ! Read and clear buffer 1
 7    OUTPUT 12 USING "#,W";0                    ! Set timer to 0
 8    OUTPUT 12 USING "#,W";Startcode            ! Start accum; swap buffers
 9    OUTPUT 12 USING "#,W";Stopcode             ! Stop accum
10    ENTER 12 USING "#,W";D(*)                  ! Read and clear buffer 2

11    OUTPUT 12 USING "#,W";Startcode            ! Start untimed accum; swap
                                                   buffers

      • • • User program during untimed accumulation

12    OUTPUT 12 USING "#,W";Stopcode             ! Stop accum

13    OUTPUT 12 USING "#,W";Startcode            ! Start accum; swap buffers
14    OUTPUT 12 USING "#,W";Stopcode             ! Stop accum
15    ENTER 12 USING "#,W";D(*)                  ! Read accum data from buffer

      ...  User program to analyze data

16    ON INTR 12,10 GOSUB Readbuffer             ! Interrupt service vector
17    OUTPUT 12 USING "#,W";1000                 ! Set timer to 1 second
18    CONTROL 12,3;Startcode                     ! Start command
19    CONTROL 12,1;1                             ! Set PCTL to start accum
20    ENABLE INTR 12;2                           ! Enable buffer interrupt

      ...  User program during timed accumulation cycles

21 Readbuffer:!                                  ! Interrupt service routine
22    CONTROL 12,3;Startcode                     ! Start command
23    CONTROL 12,1                               ! Set PCTL to start next
                                                   accum; swap buffers
24    ENTER 12 USING "#,W";D(*)                  ! Read previous accum data
                                                   from buffer

      ...  User program to save/analyze data

25    ENABLE INTR 12;2                           ! Enable buffer interrupt
26    RETURN
```

Figure 3. Example program segment for HP interface.

The second program segment is written for a DEC PDP-11 computer with a DRV-11 interface. A timed accumulation cycle using an interrupt-driven buffer read routine is illustrated. The major sections of this program example are as follows:

lines

1-6 These lines define the DRV-11 register addresses and reserve memory for a data buffer.

7-20 The lines read in the current output buffer, swap the buffers, and read in the second buffer. This clears the buffers prior to use for data accumulation.

21-23 These lines set up the address of the interrupt service routine and prepare the DRV-11 to properly generate the interrupts.

24-25 The on-board timer is set to 1 second and the first timed accumulation cycle is started.

26-36 These lines are the interrupt service routine that is called at the end of each timed accumulation cycle. Line 28 starts the next accumulation cycle and swaps the buffers. In a typical spectrometer application, for example, this routine would update the scan conditions prior to issuing this command. After the buffers have been swapped, lines 29-33 add the data from the previous accumulation cycle to the program data buffer while the newly started accumulation cycle is in progress. After

processing the data, the interrupt is re-enabled in line 35 for the current accumulation cycle.

This program can be easily modified to operate in a continuous accumulation mode. Changing the 番1000・ to f0 in line 24 sets the timer to 0. The Buffer Memory then generates an interrupt when any channel becomes completely full (65,535 counts). The interrupt service routine swaps the buffers and starts the accumulation in the other buffer. The data from the output buffer is added to that already in memory. This process continues until the user program issues a stop command (MOV #100000,@#DETOUT) to the Buffer Memory.

The program example uses interrupts to control the reading of the Buffer Memory by the host computer. The DRV-11 and DR11-C also provide the option of treating the service request as a flag rather than an interrupt. If the interrupt enable commands (lines 23 and 35 in the example program) are not included, the service request will function as a flag. The user program can check this flag by reading the control and status register and checking the value of bit 7 (REQUEST A) ・ If bit 7 has the value 1, then the Buffer Memory has requested service; i.e, a timed accumulation has completed or a memory channel is full.

```
1   DETCSR    -167750                    ; DRV-11 Control and Status register
2   DETOUT    =167752                    j DRV-11 Output register
3   DETIN     =167754                    ; DRV-11 Input register
4   DETVEC    =320                       ? Interrupt service vector address
5   DATBUF:   BLKW  8192.                ; Double word data buffer
6   BUFEND    = .

7   INIT:     NOP                        .* Initialization sequence
8             MOV     #0.,@#DETOUT       .* Set timer to 0
9             MOV     #0'R0              ; RO is input counter
10  CLR1:     MOV     @#DETIN,R1         , Read word from bufferl, clear it
11            INC     RO                 ; Increment counter
12            CMP     RO,#4096.          ; Test if done
13            BLT     CLR1               ; Repeat until done

14            MOV     #100001,@#DETOUT   ; Start accum, swap buffers
15            MOV     #100000,@#DETOUT   ,* Stop accum
16            MOV     #0,R0              ; RO is input counter
17  CLR2:     MOV     @#DETIN,R1         : Read word from buffer2, clear it
18            INC     RO                 ; Increment counter
19            CMP     RO,#4096.          ; Test if done
20            BLT     CLR2               ; Repeat until done

21            MOV     #READIN,@#DETVEC   ,* Set interrupt vector address
22            MOV     #340,@#DETVEC+2    .* Processor status during interrupt
23            MOV     #100,@#DETCSR      ; Set DRV-11 to allow interrpts

24            MOV     #1000.,@#DETOUT    ; Set timer to 1 second
25            MOV     #100001,@#DETOUT   ; Start accum, swap buffers

              . . . User program during      timed accumulation cycles

26  READIN:   NOP                        ; Interrupt service routine
27            MOV     RO,-(SP)           ; Save RO
28            MOV     #100001,@#DETOUT   , Start next accum, swap buffers
29            MOV     #DATBUF,R0         ; Set RO to point at data buffer
30  LOOP:     ADD     @#DETIN,(R0)+      ; Transfer data
31            ADC     (R0) +             ; Double word buffer
32            CMP     RO,#BUFEND         ; Test to see if done
33            BLE     LOOP               ; Repeat until done
34            MOV     (SP)+'RO           ; Restore RO
35            MOV     #100,@#DETCSR      ; Enable DRV-11 interrupt
36            RTI                        ; Exit routine
```

Figure 4. Example program segment for DEC interface.

4. MODEL 2412A BUFFER MEMORY HARDWARE INTERFACING

4.1. Position Computer Data

The Model 2412A Buffer Memory is normally installed physically within the Model 2401 Position Computer when used with this unit◦ In this configuration, the Buffer Memory is connected to the Position Computer by two internal 26-wire cables (part # 001080-00) that transfer the X and Y coordinate data. The X data cable goes from 2412A connector P2 to 2401 connector P2 ; Y data from 2412A connector Pl to 2401 connector P3. Both cables conform to the set of connections described in Table 3 below.

Table 3. Cable specifications (2412A to 2401) <,

Function	2412A • Pl 2412A - P2	2401 • P3 2401 - P2	(Y data) (X data)
bit 0	pin 1	pin 1	
bit 1	2	2	
bit 2	3	3	
bit 3	4	4	
bit 4	5	5	
bit 5	6	6	
bit 6	7	7	
bit 7	8	8	
bit 8	9	9	
bit 9	10	10	
Strobe	11	11	
Rate	12	12	
Common	13-26	13-26	

4o2o SP GPIO—Compatible Host Computer Interface

The 2412-02 or 2412-22 Buffer Memory is configured with a host computer interface compatible with the HP 98622A GPIO Interface. This interface includes a 16-bit data input bus (buffer to host), a 16-bit data output bus (host to buffer), and three data transfer control lines. Figure 5 illustrates these connections.

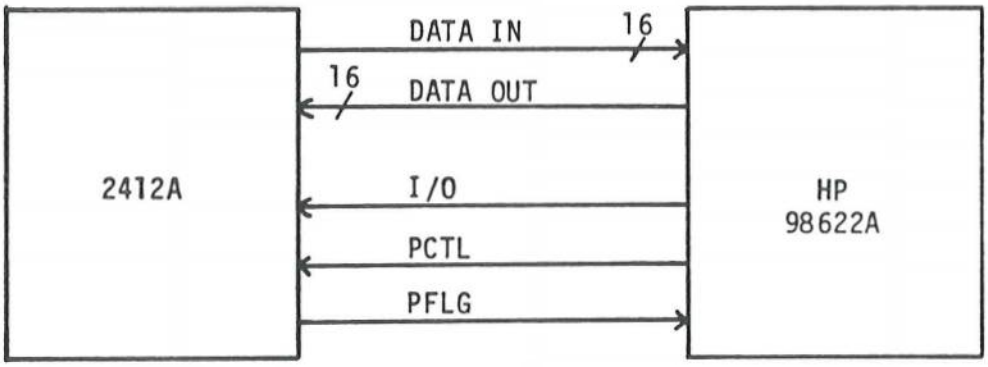


Figure 5. HP GPIO-compatible interface connections.

The Buffer Memory is connected to the host computer interface card via a single 50-wire cable from connector P5 on the 2412A board. Table 5, at the end of this section, contains a wiring specification for this cable. Note that the cable provides mirror-image connections.(pin 1 to pin 50, pin 2 to pin 49, etc.) and can be implemented using ribbon cable. The standard installation uses two cables: part # 061010-00 from the 2412A board to the 2401 back panel and part # 002045-00 from the back panel to the host.

Table 4 lists the standard settings for the Option Select and Data-In Clock Source switches on the HP 98622A GPIO card; the select

code and interrupt level switch settings are determined by the user application program requirements. The information in this section assumes that the switches are set according to these specifications.

Table 4. Standard switch settings for HP 98622A interface.

Switch:	PCTL	PFLG	PSTS	HSHK	DIN	DOUT	RD	BSY	RDY	RD	BSY	RDY
Setting:	1	0	0	1	0	0	1	1	0	1	1	0

Three control lines (I/O, PCTL, and PFLG) provide the necessary handshaking signals to transfer data between the Buffer Memory and the GPIO interface card. The paragraphs below summarize the functions of each of these lines. For additional information, refer to the HP GPIO manual.

The I/O line determines the direction of the data transfer. When this line is low, conunands are transferred from the host computer to the Buffer Memory. When this line is high, the data value from the memory location pointed to by the Buffer Memory address pointer is transferred to the host computer.

The PCTL line controls the start of a data transfer. After the host computer places the proper values on the data and I/O lines, it initiates the transfer by a TTL high-to-low transition on the PCTL line. On receipt of this transition, the Buffer Memory either accepts and acts on the command or outputs a buffer data value# depending upon the state of the I/O line. After the Buffer Memory acknowledges the command (a high-to-low PFLG transition) t the host computer return the PCTL high to the TTL high state.

The PFLG line is used as a Ready/Busy line. When this line is high, the Buffer Memory is ready to accept a command. The Buffer Memory acknowledges receipt of a command by placing the PFLG line in the low state. The line is left in the low state until the command or data transfer is complete. Typical response times for the various functions are given below:

Set Timer PFLG low time is approximately equal to PCTL low time, delayed by about 50 ns.

Read Data Up to 1 microsecond, depending upon input activity.

Stop Accum Up to 1 microsecond, depending upon input activity.

Start Accum If the timer value is non-zero, PLFG stays low until the specified time interval has elapsed. The resulting low-to-high PFLG transition is used to generate an interrupt to the host computer.

If the timer is set to zero, PFLG stays low for the same amount of time as PCTL is low, delayed by about 50 ns. A second negative PFLG pulse of approximately 150 ns will be generated if any input buffer channel becomes completely full (65,535 counts). The low-to-high transition of this second PFLG pulse is used to generate an interrupt to the host computer.

Table 5. Cable Specifications (2412A to HP GPIO interface).

Function	2412A - P5	HP GPIO
Data In bit 0	pin 9	pin 42
Data In bit 1	10	41
Data In bit 2	11	40
Data In bit 3	12	39
Data In bit 4	13	38
Data In bit 5	14	37
Data In bit 6	15	36
Data In bit 7	16	35
Data In bit 8	17	34
Data In bit 9	18	33
Data In bit 10	19	32
Data In bit 11	20	31
Data In bit 12	21	30
Data In bit 13	22	29
Data In bit 14	23	28
Data In bit 15	24	27
Data Out bit 0	34	17
Data Out bit 1	35	16
Data Out bit 2	36	15
Data Out bit 3	37	14
Data Out bit 4	38	13
Data Out bit 5	39	12
Data Out bit 6	40	11
Data Out bit 7	41	10
Data Out bit 8	42	9
Data Out bit 9	43	8
Data Out bit 10	44	7
Data Out bit 11	45	6
Data Out bit 12	46	5
Data Out bit 13	47	4
Data Out bit 14	48	3
Data Out bit 15	49	2
I/O	31	20
PCTL	32	19
PFLG	7	44
PSTS	6	45
STIO	4	47
PRESET	30	21
Conunon	50	1
Common	33	18
Common	27	24
Common	25	26
Common	2	49

Note this cable may be implemented as a mirror-image ribbon cable.

4 □ 3» DEC—Compatible Host Computer Interface

The 2412-01 or 2412-21 Buffer Memory is configured with a host computer interface compatible with DEC DRV-11 and DR-11C General Device Interfaces. The interface includes a 16-bit data input bus (buffer to host)$_t$ a 16-bit data output bus (host to buffer), and three data transfer control lines. Figure 6 illustrates these connections.

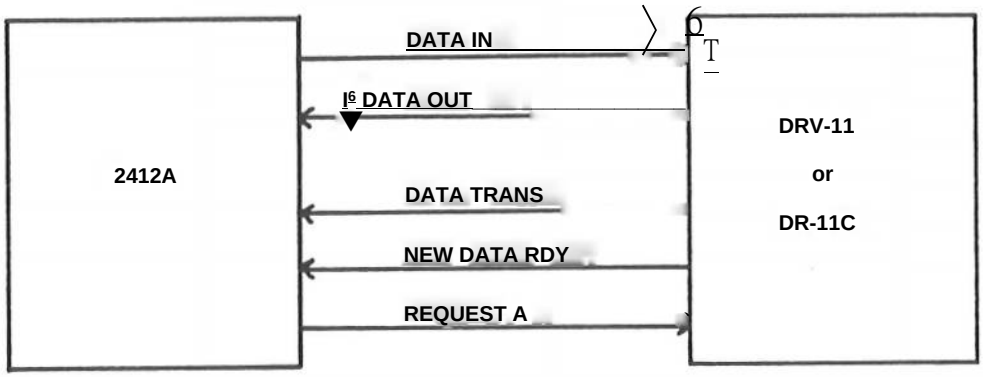


Figure 6. DEC-compatible interface connections.

The Buffer Memory is connected to the interface card via two 40-wire cables; the first goes from connector P3 on the 2412A board to connector No.2 on the interface card, the second from P4 on the 2412A to connector No.1 on the interface. Table 6, at the end of this section, contain wiring specifications for these cables. The cables may be implemented as 40-conductor ribbon cables. The standard installation replaces each of these cables by two cables: part # 001071-00 from the 2412A board to the 2401 back panel and part # 001072-00 from the back panel to the host.

The register addresses and interrupt level of the DRV-11 or DR-11C interface are determined by jumpers on the interface board. If necessary, these should be changed by the user to correspond to the values used in the host computer program.

The interface card also must be modified by adding a 1500 pF capacitor to lengthen the DATA TRANS pulse. This allows the circuitry to access the Buffer Memory data (with queuing delays) and present it at the output in one processor step. The added capacitor will result in a pulse width of about 1 microsecond. Install the capacitor at the terminals provided on the interface card (between back panel pin EB1 and ground)·

Three control lines (DATA TRANS, NEW DATA RDY, and REQUEST A) provide the necessary handshaking signals to transfer data between the Buffer Memory and the DEC interface card. The paragraphs below summarize the functions of each of these lines. For additional information, refer to the DRV-11 or DR-11C manual.

The DATA TRANS line controls the reading of data from the Buffer Memory. A positive pulse on this line transfers the word from the output buffer location pointed to by the Buffer Memory address pointer to the host computer. The address pointer is then incremented so that a subsequent pulse will transfer the next data value.

The NEW DATA RDY line controls the transfer of data from the host computer to the Buffer Memory. On the high-to-low transition of a positive pulse on this line, accepts and acts on the command on the data

output (host to buffer) bus.

The REQUEST A line is used by the Buffer Memory to request service from the host computer. This line is placed in the high state upon the completion of a timed accumulation cycle or if any input buffer channel becomes completely full (65,535 counts) during an untimed accumulation. A high level on this line is used as a flag or to generate an interrupt, depending upon how the interface card was programmed by the user software.

Table 6◦ Cable Specifications (2412A to DEC interface).

Function	2412A - P3	DRV-11/DR-11C Connector 2
Data In bit 0	pin TT	pin TT
Data In bit 1	LL	LL
Data In bit 2	H_rE	H,E
Data In bit 3	BB	BB
Data In bit 4	KK	KK
Data In bit 5	HH	HH
Data In bit 6	EE	EE
Data In bit 7	CC	CC
Data In bit 8	Z	Z
Data In bit 9	Y	Y
Data In bit 10	W	W
Data In bit 11	V	V
Data In bit 12	u	U
Data In bit 13	p	P
Data In bit 14	N	N
Data In bit 15	M	M
DATA TRANS	C	C
Common	J ,L'R , T,X,AA, DD_rJJ_r MM'PP, SS_rUU	J ,L ,R , T.X-AA. DD,JJ, MM,PP, SS_rUU

Table 60 continued ,

Function	DRV-11/DR-11C 2412A - P4 Connector 1	pin C
Data Out bit 0	pin C	K
Data Out bit 1	K	NN.RR
Data Out bit 2	NN$_r$RR	U
Data Out bit 3	U	L
Data Out bit 4	L	N
Data Out bit 5	N	R
Data Out bit 6	R	T
Data Out bit 7	T	W
Data Out bit 8	W	X
Data Out bit 9	X	Z
Data Out bit 10	Z	AA
Data Out bit 11	AA	BB
Data Out bit 12	BB	FF
Data Out bit 13	FF	HH
Data Out bit 14	HH	JJ
Data Out bit 15	JJ	W
NEW DATA RDY	W	LL
REQUEST A	LL	P
INIT	P	J,M,S, V,Y,CC$_r$ EE$_r$KK$_r$ MM'PP, SS$_r$UU
Common	J,M,S, V,Y,CC, EE$_r$KK$_r$ MM'PP, SS$_r$UU	

Appendix A

MODIFYING THE X-Y INPUT MAPPING CONNECTIONS

Section 2.2 of this manual described the use of the X-Y input connections to map specific regions on the sensor into input and output buffer channels. This appendix is intended as a guide for users needing to modify the factory-wired default configuration to meet their own requirements.

The X-Y input mapping is defined by a set of wire-wrap connections on the Model 2412A Buffer Memory board. Five wire-wrap terminal strips are provided, located near the P1 and P2 connectors. Figure A-1 shows the layout, with the individual pins labeled for reference. Note that these labels are not actually present on the Buffer Memory board, but are added to simplify the following instructions. The five wire-wrap terminal strips are as follows:

X A set of 10 pins adjacent to the P2 connector. These lines contain the X coordinate data from the Position Computer.

Y A set of 10 pins adjacent to the P1 connector. These lines contain the Y coordinate data from the Position Computer.

GND A set of 3 pins connected to logic ground. These are provided as convenient tie points for connecting unused address inputs to ground.

A A set of 7 pins and a set of 5 pins. These lines are the 12 bits of the Buffer Memory channel address. Unused address pins must be connected to GND.

The choice of address mapping will vary according to the application. It may be useful to refer back to the information in Section 2.2 relating sensor positions to X and Y coordinates and buffer addresses. In order to simplify the software required to read and analyze the data and to ensure consistent Buffer Memory operation, the following guidelines should be followed in determining the address mapping connections for a specific application.

1) Fewer than 12 bits may be used to form the channel address. If so, the selected X and Y input lines must be connected to the low order Buffer Memory address bits (A_Q - A_n). The remaining high order address bits ($A_{n+}j$ - A_{11}) must be connected to GND. This assignment ensures that the data is stored in a single contiguous block starting at buffer address 0.

2) The number of address lines chosen from the X and Y inputs is arbitrary, but the total number of lines from X and Y cannot exceed 12. If the Position Computer has digital outputs for only the Y axis (Model 2401 Option EB or EH), then only Y input lines may be chosen.

3) If only some of the address lines from an input (X or Y) are used, then the lines selected should be a contiguous set of high order bits. For example, if 4 bits of the X input are to be included, then the bits selected would be X_4 - X_7 for an 8-bit resolution system and

X6 " x9 f°r a 10-bit resolution system«»

4) The selected X bits should be connected, in order, to a contiguous set of address lines. Similarly for the selected Y bits• The choice of whether the X or Y bits become the low order channel address bits is arbitrary, however it will affect the user software for analyzing the data.

The remainder of this appendix describes several common X-Y input mappings. For each example, the proper wire-wrap connections and the relationship between channel number and X-Y coordinates are given. This is by no means an exhaustive list of input combinations, but is intended to be representative of common application requirements◦

Example !• Default configuration (factory-wired). 8-bit resolution system, 4 bits X data, 8 bits Y data.

Wire-Wrap Connections		Buffer Channel Assignments		
Position Computer	Channel Address	Channel Number	Position Coordinates X	Y
Y_0	A_0	0	0-15	0
Y_1	A_1	1	0-15	1
Y_2	A_2	• • •	• • •	
Y_3	A_3	254	0-15	254
Y_4	A_4	255	0-15	255
Y_5	A_5	256	16 - 31	0
Y_6	A_6	257	16 - 31	1
Y_7	A_7	- • •	• 參 •	
X_4	A_8	3838	224 - 239	254
X_5	A_9	3839	224 - 239	255
X_6	A_{10}	3840	240 - 255	0
X_7	A_{11}	3841	240 - 255	1
		• • •	• • •	
		4094	240 - 255	254
		4095	240 - 255	255

Example 2. 10-bit resolution system, 10 bits Y data, no X data.
For an 8-bit resolution system, A_0 and Ag would be connected to GND instead of Y_0 and Yg as shown.

Wire-Wrap Connections		Buffer	Channel Assignments	
Position Computer	Channel Address	Channel Number	Position Coordinates X	Y
Y_0	A_0	0	0 — 1023	0
Y_1	A_1	1	0 - 1023	1
Y_2	A_2	...	...	
Y_3	A_3	255	0 - 1023	255
Y_4	A_4	256	0 - 1023	256
Y_5	A_5	...	...	
Y_6	A_6	1022	0 - 1023	1022
Y_7	A_7	1023	0 - 1023	1023
Y_8	A_8			
Y_9	A_9	1024		
GND	$\overline{M}10$	...	not used	
GND	A_{11}	4095		

Exaaple 3. 8-bit resolution system, 7 bits X data, no Y data.

Wire-Wrap Connections

Position Channel Computer Address	
X_1	A_0
X_2	A_1
X_3	A_2
X_4	A_3
X_5	A_4
X_6	A_5
X_7	A_6
GND	A_7
GND	A_8
GND	A_9
GND	A_{10}
GND	A_{11}

Buffer Channel Assignments

Channel Number	Position Coordinates X	Y
0	0 - 1	0 - 255
1	2-3	0 — 255
...	...	
126	252 - 253	0 - 255
127	254 - 255	0 - 255
128		
...	not used	
4095		

Exa^ple 4. 8-bit resolution system, 6 bits X data, 6 bits Y data.
This configuration provides image elements with equal dimensions on both sensor axes.

Wire-Wrap Connections		Buffer Channel Assignments		
Position Computer	Channel Address	Channel Number	Position Coordinates X	Y
Y_2	A_0	0	0-3	0-3
Y_3	A_1	1	0-3	4-7
Y_4	A_2	• • •	o o •	
Y_5	A_3	62	0-3	248 _ 251
Y_6	A_4	63	0-3	252 - 255
Y_7	A_5	64	4-7	0-3
X_2	A_6	65	4-7	4-7
X_3	A_7	• • •	o • •	
X_4	A_8	4030	248 - 251	248 - 251
X_5	A_9	4031	248 - 251	252 - 255
X_6	A_{10}	4032	252 - 255	0-3
X_7	A_{11}	4033	252 - 255	4-7
		• ..	• *»	
		4094	252 • 255	248 - 251
		4095	252 - 255	252 - 255

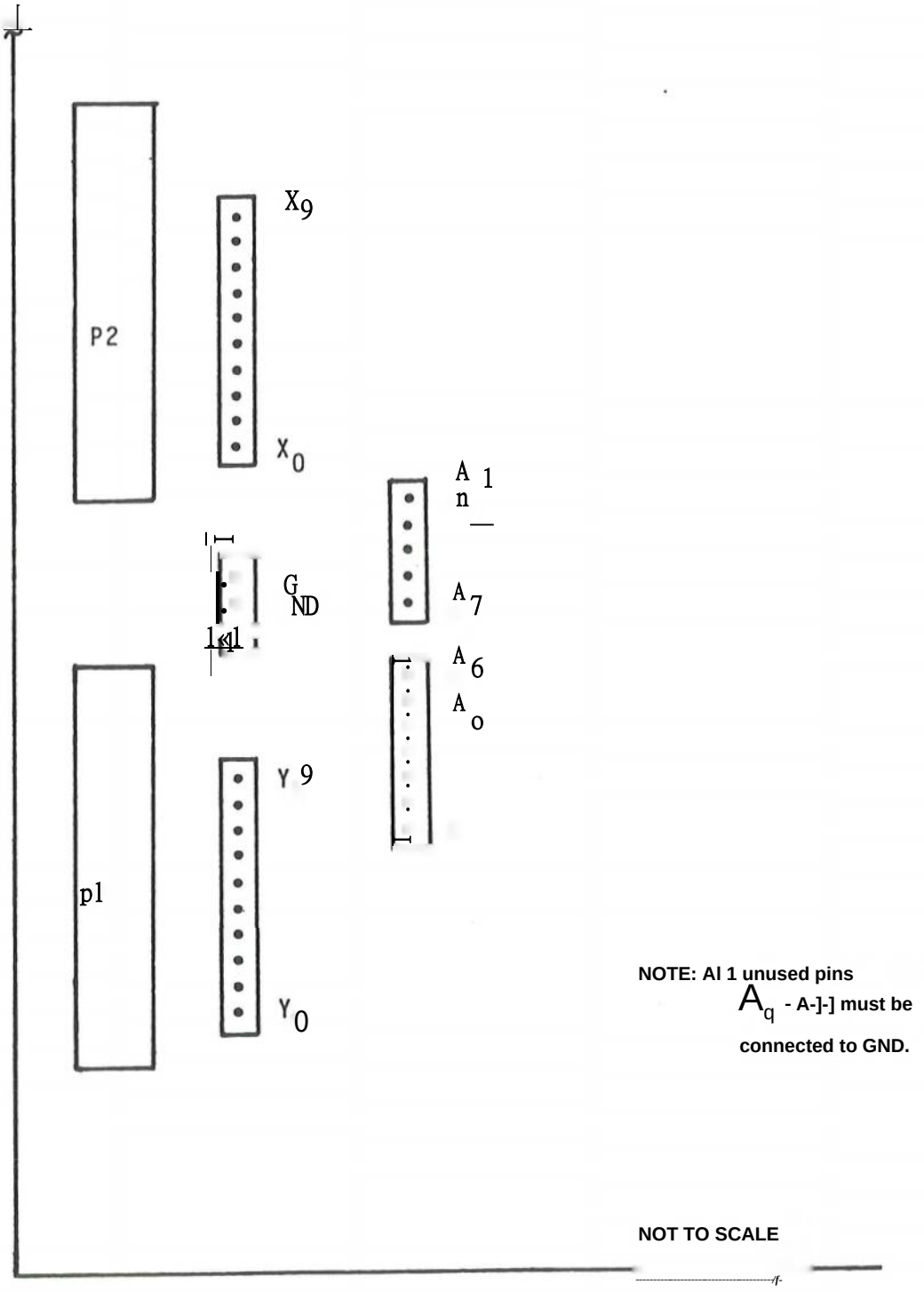


Figure A-1. X-Y input mapping wire-wrap terminals.

Appendix B

FIELD INSTALLATION OF THE MODEL 2412A BUFFER MEMORY

B.l. General Information

The Model 2412A Buffer Memory is typically shipped from the factory installed in the Model 2401 Position Computer. This appendix describes the procedure for the user to field-install the 2412A board in an existing Model 2401 Position Computer. The 2401 must be equipped with digital outputs (Option EB, EC, EH, or EJ) for either one or both axes. If digital outputs exist for only one axis, then only output from that axis can be used as input to the buffer memory (Appendix A).

Alternatively, the Buffer Memory may be installed in an enclosure of the user's design. A power supply must be provided (5 VDC ± 5% at 1.0 Amp). This method is appropriate for use with a Model 2391 Position Computer (which cannot physically accomodate the Model 2412A).

B.2. Installation of 2412-21 (DEC compatible) in Model 2401

This section describes the procedure for customer field installation of the 2412-21 (DEC interface) into an existing Model 2401 Position Computer. All of the required hardware and cables for installing the Buffer Memory are provided with the 2412-21. Table B-1 lists the contents of the installation and cable kits for the DEC compatible Buffer Memory.

Table B-1. 2412A Installation and Cable Kits (DEC compatible).

Item	2£y	Part #	Description
	1	001638-00	Installation Kit, consists of:
1	4	4500-0013	Screw, 4-40 x .750'*
2	1	3166-0018	Plug housing, AMP 102241-4
3	2	3166-0019	Socket pins$_r$ AMP 87523-7
4	1	002098-00	Labels "JI"
5	1	002099-00	Label: "J2"
6	1	002100-00	Label: "2412 Installed'*
7	1	9000-0460	2412A manual
	1	002097-00	Cable Kit, consists of:
8	2	001080-00	Cable$_z$ 26-conductor flat' 5"
9	2	001071-00	Cable, 40-conductor flat, 12"
10	2	001072-00	Cable, 40-conductor flat, 3 meter

Installation Instructions

1. Be certain the 2401 is disconnected from the power source. Remove the top and bottom covers from the 2401 case. Figure B-1 (at the end of this Appendix) identifies the parts on the 2401 printed circuit board and indicates where the 2412A board will be mounted.

2. Disconnect the 26-wire flat cables from P2 and P3 on the 2401 board and remove the X-axis Digital Output and Y-axp Digital Output

connectors on the 2401 back panel. (If the 2401 has digital outputs on only one axis, then only one cable will be present.)

3. Remove the blank cover' if present, from the X-axis Digital Output cutout in the 2401 back panel.

4. Remove (from the bottom) the 4 short bolts holding the 2401 board in place. These locations are identified as (A) and ⑧ in Figure B-1. Replace these bolts with the longer bolts supplied (item 1); the threads will extend through the 2401 circuit board. Installation of the pivot stand-offs in step 6 will be easier if the stand-offs on the 2401 board in location ⑧ are drilled through with a 1/8'* bit before installing the longer bolts.

5. Remove the 2 hex stand-offs and 2 pivot stand-offs from the 2412A board. Screw the hex standoffs onto the bolts at locations ⑧ in Figure B-1 until tight.

6. Screw the pivot stand-offs onto the bolts at locations ⑧ in Figure B-1 until tight, then back off until the top section of the stand-off pivots from the front to back, parallel to the sides of the 2401 case.

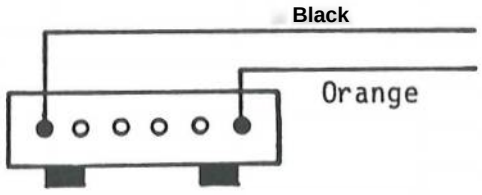
7. Attach the 2412A board to the pivot stand-offs, then to the hex • stand-offs.

8. Install the 5", 26-conductor flat cables (item 8) from a) P2 on the 2401 board to P2 on the 2412A board, and b) P3 on the 2401 board to Pl on the 2412A board. Note that the stripe on each cable should

be on the left side, as viewed from the front of the 2401 box.

9. Attach the 50-pin D connector on the 12", 40-conductor cable (item 9) to the Y-axis Digital Output cutout in the 2401 backpanel using the hardware supplied. Plug the 40-pin header into P3 on the 2412A board. Repeat using the second cable, the X-axis Digital Output cutout, and P4. Note that the stripe on each cable should be on the right side, as viewed from the front of the 2401 box.

10. Cut the cable tie holding the power wires (near location ⑧ on the right side of Figure B-1) already installed in the 2401 box. Crimp or solder the socket pins (item 3) onto the ends of these wires and install the pins in the power plug housing (item 2) • Note the orientation of these pins, as shown below:



(top view)

11. Insert the power plug into P6 on the 2412A board. Verify that the black wire is closest to P1 and P2. The 2401 with the 2412A installed should now appear as illustrated in Figure B-2.

12. Replace the top and bottom covers of the 2401 box.

13. Install the labels (items 4-6) on the back panel of the 2401 as follows. The "J1" label should be placed on top of the existing "X axis digital output" labeling and "J2" on top of the "Y axis

digital output" labeling. The *'2412 installed11 label should be placed in the blank area on the left side of the back panel.

14. Connect the long 40-conductor cables (item 1) from the back panel of the 2401 to the corresponding connectors on the DEC interface, Plug the 2401 into the power source and verify proper system operation.

Bo3. Installation of 2412-22 (HP compatible) in Model 2401

This section describes the procedure for customer field installation of the 2412-22 (HP interface) into an existing Model 2401 Position Computer. All of the required hardware and cables for installing the Buffer Memory are provided with the 2412-22. Table B-2 lists the contents of the installation and cable kits for the HP compatible Buffer Memory.

Table B-2. 2412A Installation and Cable Kits (HP compatible).

Item	Qty	Part #	Description
	1	001637-00	Installation Kit, consists of:
1	4	4500-0013	Screw, 4-40 x .750"
2	1	3166-0018	Plug housing, AMP 102241-4
3	2	3166-0019	Socket pins, AMP 87523-7
4	1	026409-00	Blank cover plate
5	2	4500-0001	Screw, 6-32 x .250"
6	1	002101-00	Label: "HP GPIO"
7	1	002100-00	Label: **2412 Installed"
8	1	9000-0460	2412A manual
	1	002097-00	Cable Kit, consists of:
9	2	001080-00	Cable, 26-conductor flat, 5"
10	1	061010-00	Cable, 50-conductor flat, 12"
11	1	002045-00	Cable, 50-conductor flat, 3 meter

Installation Instructions

1. Be certain the 2401 is disconnected from the power source. Remove the top and bottom covers from the 2401 case. Figure B-1 (at the end of this Appendix) identifies the parts on the 2401 printed circuit board and indicates where the 2412A board will be mounted.

2. Disconnect the 26-wire flat cables from P2 and P3 on the 2401 board and remove the X-axis Digital Output and Y-axis Digital Outgut connectors on the 2401 back panel. (If the 2401 has digital outputs on only one axis, then only one cable will be present.)

3. Install the blank cover (items 4,5) over the X-axis Digital Output cutout on the 2401 back panel. If the 2401 has digital outputs on only one axis, this cover may already be in place.

4. Remove (from the bottom) the 4 short bolts holding the 2401 board in place. These locations are identified as ⑧ and ⑨ in Figure B-1. Replace these bolts with the longer bolts supplied (item 1); the threads will extend through the 2401 circuit board. Installation of the pivot stand-offs in step 6 will be easier if the stand-offs on the 2401 board in location ⑨ are drilled through with a 1/8" bit before installing the longer bolts.

5. Remove the 2 hex stand-offs and 2 pivot stand-offs from the 2412A board. Screw the hex standoffs onto the bolts at locations (A) in Figure B-1 until tight.

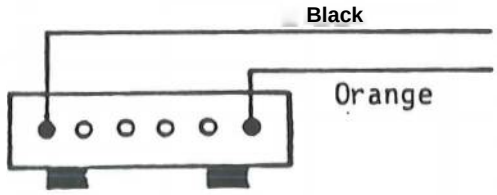
6. Screw the pivot stand-offs onto the bolts at locations ⑨ in Figure B-1 until tight, then back off until the top section of the stand-off pivots from the front to back, parallel to the sides of the 2401 case.

7. Attach the 2412A board to the pivot stand-offs, then to the hex stand-offs.

8. Install the 5", 26-conductor flat cables (item 9) from a) P2 on the 2401 board to P2 on the 2412A board, and b) P3 on the 2401 board to P1 on the 2412A board. Note that the stripe on each cable should be on the left side, as viewed from the front of the 2401 box.

9. Attach the 50-pin D connector on the 12", 50-conductor cable (item 10) to the Y-axis Digital Output cutout in the 2401 backpanel using the hardware supplied. Plug the 50-pin header into P5 on the 2412A board. Note that the stripe on the cable should be on the left side, as viewed from the front of the 2401 box.

10. Cut the cable tie holding the power wires (near location ⑧ on the right side of Figure B-1) already installed in the 2401 box. Crimp or solder the socket pins (item 3) onto the ends of these wires and install the pins in the power plug housing (item 2) • Note the orientation of these pins, as shown below:



(top view)

11. Insert the power plug into P6 on the 2412A board. Verify that the black wire is closest to P1 and P2. The 2401 with the 2412A installed should now appear as illustrated in Figure B-2$_r$ except there should be a single cable from connector P5 to a 50-pin connector on the 2401 back panel instead of the two cables shown from P3 and P4.

12. Replace the top and bottom covers of the 2401 box.

13. Install the labels (items 6,7) on the back panel of the 2401 as follows. The "HP GPIO'* label should be placed on top of the existing "Y axis digital output" labeling. The "2412 installed" label should be placed in the blank area on the left side of the back panel.

14. Connect the long 50-conductor cable (item 11) from the back panel of the 2401 to the corresponding connector on the HP GPIO interface. Plug the 2401 into the power source and verify proper system operation.

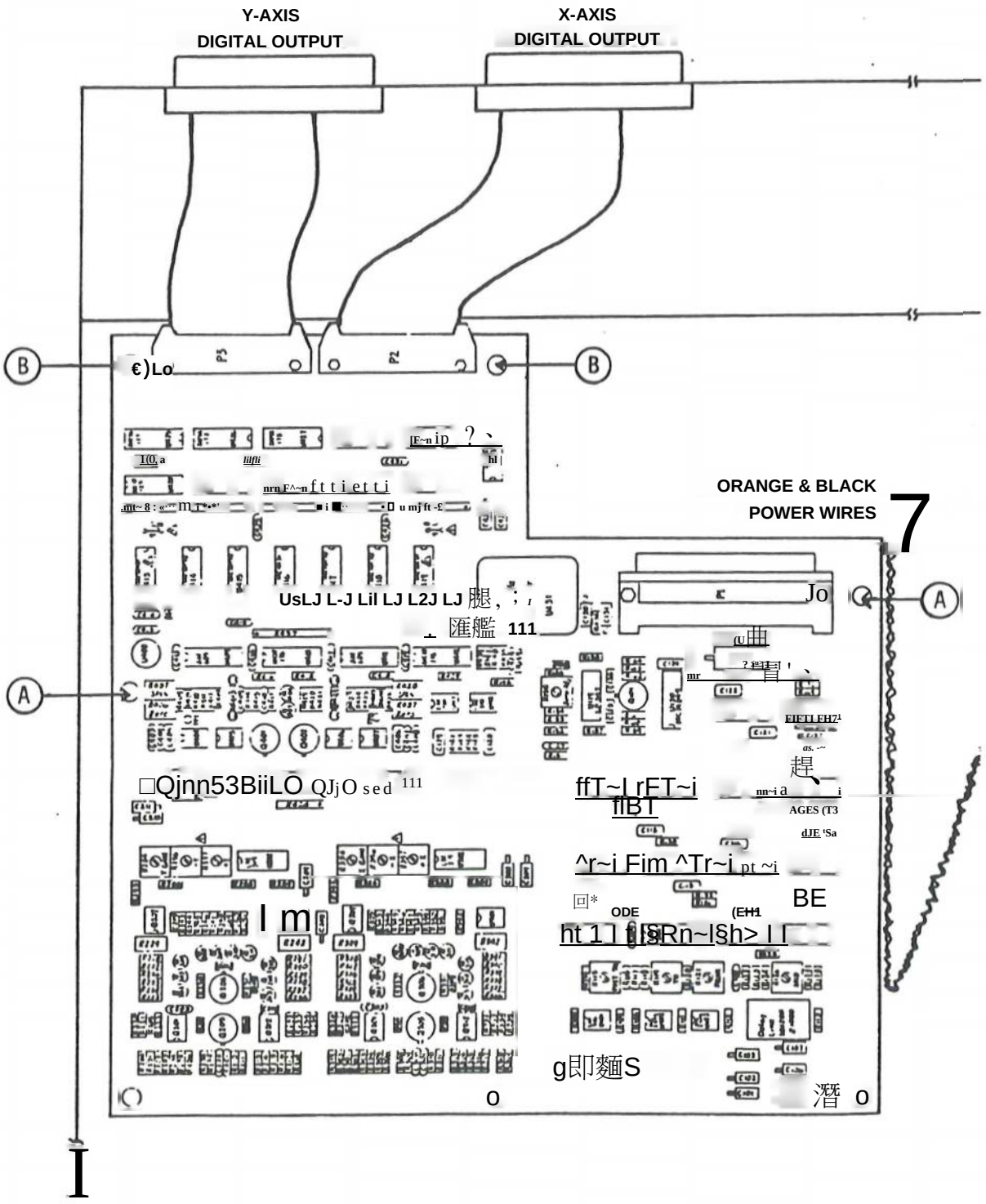


Figure B-1. 2401 parts layout showing 2412A mounting locations.

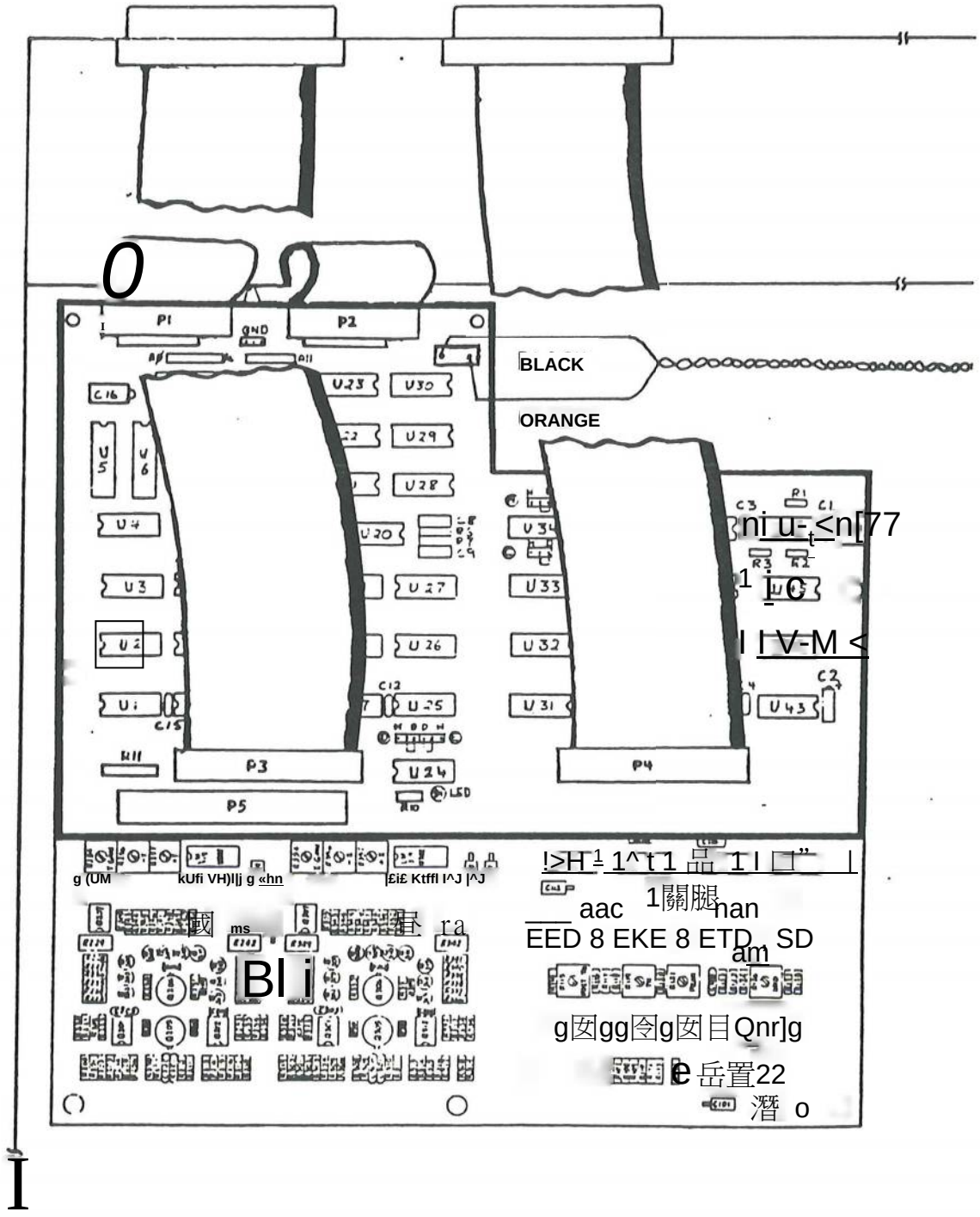


Figure B-2. 2412A Buffer Memory installed in 2401 Position Computer.

Appendix C

TECHNICAL DATA

C.l. 2412A Part Numbers Summary

This section sununarizes the SSI part numbers for various configurations and major components of the Model 2412A Buffer Memory. A parts list for the 2412A printed circuit board is included in the following section.

Part Number	Description
2412-01	Buffer Memory installed in Model 2401 Position Computer ; DEC compatible interface
2412-02	Buffer Memory installed in Model 2401 Position Computer ; HP GPIO compatible interface
2412-21	Buffer Memory ; DEC compatible interface
2412-22	Buffer Memory ; HP GPIO compatible interface
9000-0460	Manual, 2412A Operation and Installation
001638-00	2412 Installation Kit ; DEC compatible
001637-00	2412 Installation Kit; HP compatible
002097-00	2412 Cable Kit ; DEC compatible
002102-00	2412 Cable Kit ; HP compatible
001080-00	Cable, 26 conductor flat, 5**
001071-00	Cable, 40 conductor flat, 12"
001072-00	Cable, 40 conductor flat, 3 meter
061010-00	Cable, 50 conductor flat, 12"
002045-00	Cable, 50 conductor flat, 3 meter

C.2. 2412A Printed Circuit Board

This section includes a parts list, component layout diagrams, and schematics for the Model 2412A Buffer Memory printed circuit board. Actual boards may differ slightly due to the presence or absence of optional components and possible circuit revisions.

Table C-1 is a complete parts list for the Model 2412A printed circuit board, with differences between the HP-compatible and DEC-compatible interfaces noted.

Figure C-1 is a component layout, with jumper placement indicated.
and Figure C-3 is < a schematic of the HP-compatible Model 2412A.

Figure C-2 is a component layout, with jumper placement indicated, and Figure C-4 is a schematic of the DEC-compatible Model 2412A.

Table C-1. Model 2412A printed circuit board parts list.

Reference Designator	Part Number	Qty	Description
C1	0310-0013	1	Capacitor, 27pF$_r$ 200V
C2	0340-0001	3	Capacitor, 3.3uF, 15V, tantalum
C3 - C7	0312-0012	11	Capacitor, .022uF, 50V, disc
C8 — C9	0300-0102	2	Capacitor, 680pF, mica
CIO - C13	0312-0012		Capacitor, .022uF, 50V, disc
C14	0340-0001		Capacitor, 3.3uF$_r$ 15V, tantalum
C15	0312-0012		Capacitor, .022uF, 50V, disc
C16	0340-0001		Capacitor, 3.3uF$_r$ 15V, tantalum
C17	0312-0012		Capacitor, .022uF$_r$ 50V$_r$ disc

Table C-1. continued.

Reference Designator	Part Number	Qty	Description
LED	0820-3301	1	Light-emitting diode
P1 - P2	3135-0008	2	Connector, Ansley 609-2627
P3 - P4	3135-0009	2 [1]	Connector, Ansley 609-4027
P5	3135-0010	1 [2]	Connector, Ansley 609-5027
P6	3100-0062	1	Connector, AMP 102202-3
R1	0512-1001	1	Resistor, 1K
R2	0512-2101	1	Resistor, 2.1K
R3	0512-3011	1	Resistor, 3.01K
R4 - R5	0570-0003	2 [3]	Resistor pack, 8 x 220/330 ohm
R6	0512-7501	1	Resistor, 7.5K
R7	0512-2871	1	Resistor, 2.87K
R8 - R9	0512-1002	2	Resistor, 10K
RIO	0512-3300	1	Resistor, 330 ohm
R11	0570-0002	1	Resistor pack, 4 x 220/330 ohm
XI	0390-0001	1	Crystal, 10 MHz
U1 - U2	1011-0173	12	IC, 74LS173, Quad D register
U3	1011-0283	4	IC, 74LS283, 4 bit binary adder
U4	1014-0002	1	IC, 74HC4040, 12 stage counter
U5 - U6	1011-0244	2	IC, 74LS244, Octal line driver
U7 - U8	1011-0173		IC, 74LS173, Quad D register
U9	1011-0283		IC, 74LS283, 4 bit binary adder
U10	1050-0001	2	IC, HM6264, 8Kx8 CMOS static RAM
U11	1050-0002	2	IC, 74ALS574, Octal D flip-flop
U12 - U13	1011-0173		IC, 74LS173, Quad D register
U14	1011-0283		IC, 74LS283, 4 bit binary adder
U15	1050-0001		IC, HM6264, 8Kx8 CMOS static RAM
U16	1050-0002		IC, 74ALS574, Octal D flip-flop
U17 - U18	1011-0173		IC, 74LS173, Quad D register
U19	1011-0283		IC, 74LS283, 4 bit binary adder
U20	1012-0002	1	IC, 96S02, Dual mono multivibrator
U21	1010-0074	2	IC, 74F74, Dual D flip-flop
U22	1010-6117	1	IC, 74F00, Quad 2-in NAND
U23	1011-0074	3	IC, 74LS74, Dual D flip-flop
U24	1010-0365	1	IC, 74365, Hex buffer
U25	1011-0004	3	IC, 74LS04, Hex inverter

Table C-1. continued.

Reference Designator	Part Number	Qty		Description
U26	1011-0014	2		IC, 74LS14, Hex Schmitt Trigger
U27	1011-0074			IC, 74LS74, Dual D flip-flop
U28	1010-6118	1		IC, 74F02, Quad 2-in NOR
U29	1011-0074		[4]	IC, 74LS74, Dual D flip-flop
U30	1011-0014			IC, 74LS14, Hex Schmitt Trigger
U31	1011-0173			IC, 74LS173, Quad D register
U32	1011-0191	4		IC, 74LS191, Sync binary counter
U33	1011-0074			IC, 74LS74, Dual D flip-flop
U34	1011-0004			IC, 74LS04, Hex inverter
U35	1011-0173			IC, 74LS173, Quad D register
U36	1011-0191			IC, 74LS191, Sync binary counter
U37	1011-0151	2	[2]	IC, 74LS151, 8-to-1 multiplexer
U38	1011-0000	1		IC, 74LS00, Quad 2-in NAND
U39	1011-0173			IC, 74LS173, Quad D register
U40	1011-0191			IC, 74LS191, Sync binary counter
U41	1011-0390	2		IC, 74LS390, Dual decade counter
U42	1011-0151		[2]	IC, 74LS151, 8-to-1 multiplexer
U43	1011-0173			IC, 74LS173, Quad D register
U44	1011-0191			IC, 74LS191, Sync binary counter
U45	1011-0390			IC, 74LS390, Dual decade counter
U46	1011-0004			IC, 74LS04, Hex inverter

Notes:

[1] P3, P4 optional on HP-compatible board.

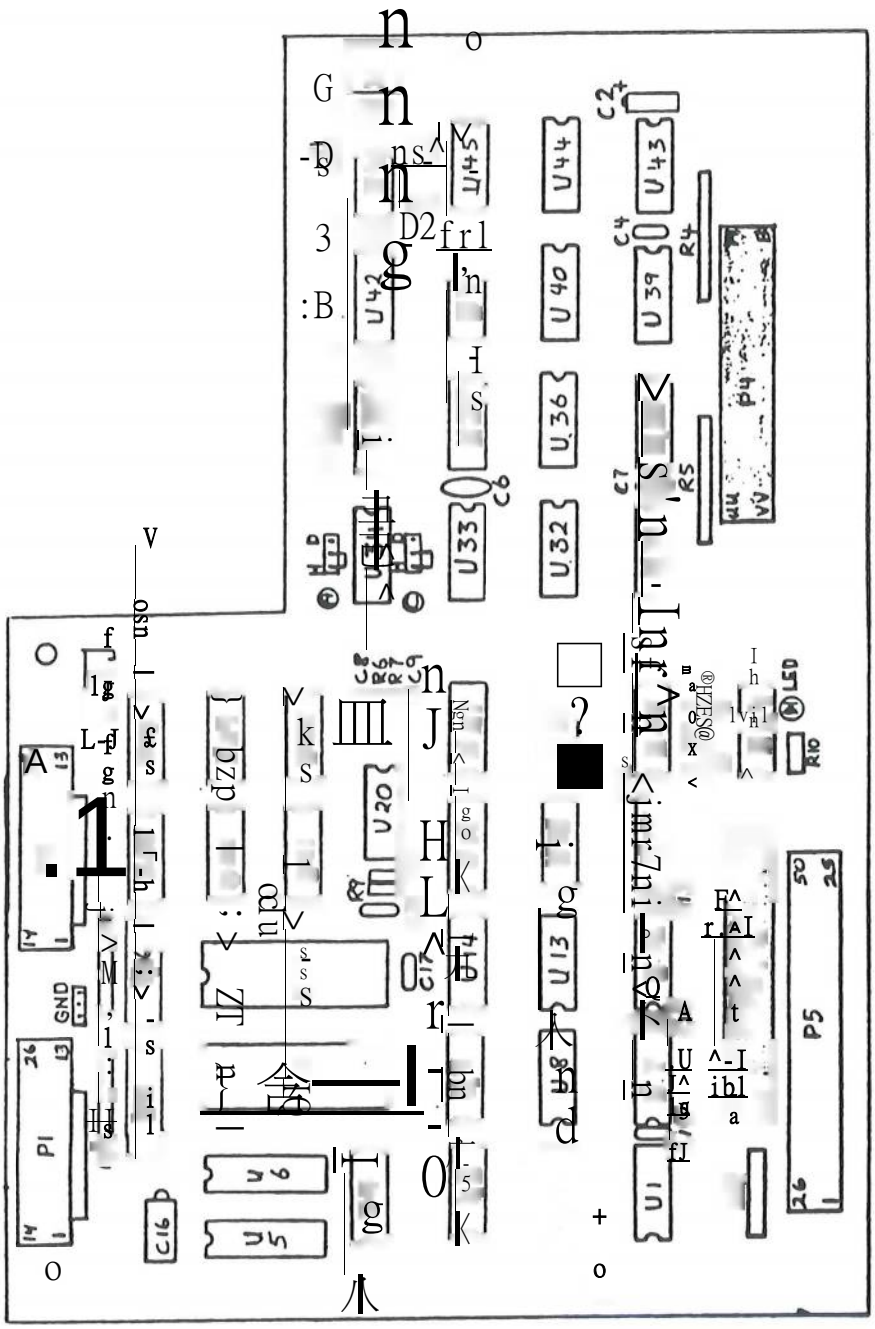
[2] P5, U37, U42 optional on DEC-compatible board.

[3] R4, R5 on HP-compatible board only.

[4] U29 (74F74) is replaced by a 74LS74 on some older boards.

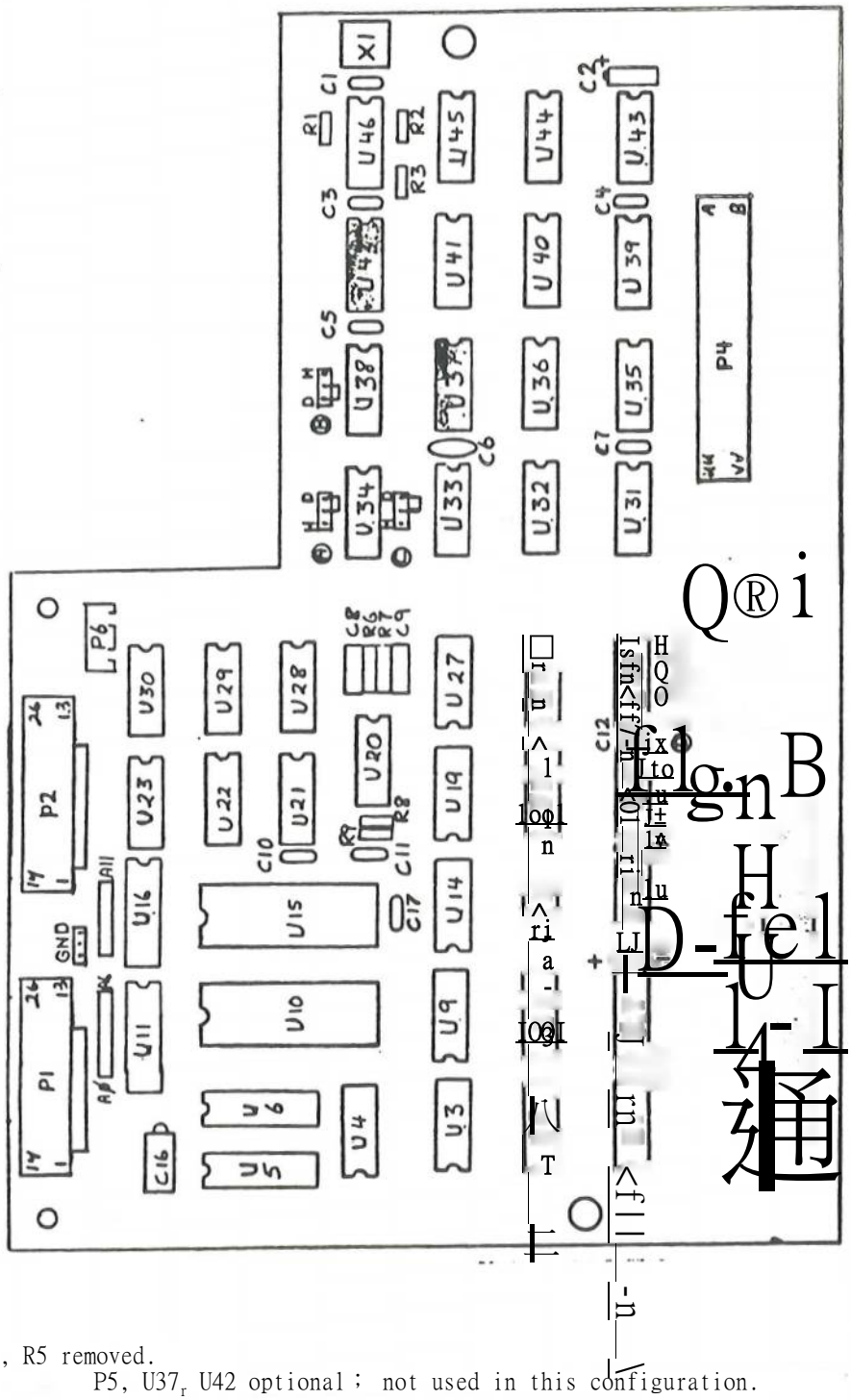
Mating connectors:

P1	-P2	Ansley 6092630
P3	-P4	3M 3417-6040
P5		Ansley 6095030
P6		AMP 102241-4 connector housing AMP 87523-7 socket pins (2 each)



Notes: P3, P4 optional; not used in this configuration.

Figure C-1. Model 2412A (HP-compatible) parts layout.



Notes: R4, R5 removed.
P5, U37, U42 optional; not used in this configuration.

Figure C-2. Model 2412A (DEC-compatible) parts layout.

Appendix D

ENGINEERING SUPPORT NOTES

Note 卷1

Date： January 1986

Subject: Change in U29 specification

A problem has been noted where simultaneous input and output requests result in spurious counts in the buffer memory. The solution is to replace the 74LS74 used as U29 by a 74F74. The problem is due to marginal timing on the slower LS part. New buffer memories will be manufactured using the 74F74.

The 74LS74 works correctly in most cases. thus users may not observe any problem with existing buffer memories. Users observing the above behavior should contact the manufacturer to arrange for an upgrade.

Note $2

Date: July 1986

Subject: Terminating shield on DEC interface cables

The cables provided for use with DEC compatible buffer memories use shielded ribbon cables to minimize interference. However, the current version of the 2412A printed circuit board does not terminate the shield to ground. Termination can be provided by connecting pin A of P3 and P4 on the 2412A board to ground. This modification will be included in a future revision of the board.

Users with older versions of the board can provide suitable termination by adding wire jumpers on the back of the printed circuit board from pin A of P3 and P4 to a nearby ground path.